IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner:	Michael Trinh
Serial No.:	09/256,643	Group Art Unit:	2822
Filed:	February 23, 1999	Docket:	303.324US2
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE		

#B Recon 10180

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on July 5, 2000. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please cancel claims 22, 25, 27, and 28 and amend the following claims:

C1

21. [Twice Amended]A method of fabricating a transistor in a semiconductor substrate, the method comprising:

forming a source region and a drain region in a semiconductor substrate, a channel region being between the source region and the drain region;

forming an insulating layer on the channel region; [and]

forming a gate on the insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$; and

selecting x [at a predetermined value approximately] to be between 0 and 1.0.

C2

23. [Amended] The method of claim [22] 21, wherein [the selected value of x establishes the desired value of the] x is selected such that a barrier energy between the gate and the insulator is [approximately] between 0 eV and 2.8 eV.

24. [Amended] The method of claim 21, wherein x is selected at a predetermined value that is [approximately] between 0.5 and 1.0.